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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/038,478 | 12/31/2001 | Joseph P. Bratt | 04860.P2693 | 7409 |

7590 08/20/2004

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| EXAMINER | |
|---|---|
| O BRIEN, BARRY J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/038,478 | BRATT ET AL. | |
| | Examiner | Art Unit | |
| | Barry J. O'Brien | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 December 2001 and 03 June 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20011231*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-48 have been examined.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 12/31/2001, Extension of Time as received on 6/03/2002 and Declaration and Fee as received on 6/03/2002.

### *Information Disclosure Statement*

3. The information disclosure statement filed 12/31/01 fails to comply with 37 CFR 1.98(a)(1), which requires a list of all patents, publications, or other information submitted for consideration by the Office. The cited reference "*Proposed SMPTE Standard for Television, SMPTE314M*" does not include a publication date. It has been placed in the application file and has been considered, but the Applicant is required to submit a publication date in response to this office action.

### *Specification*

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

### *Claim Objections*

6. Claims 2 and 20 are objected to because of the following informalities:

a. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim. A claim that depends from a dependent claim should not be separated by any claim that does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n). See claims 11-24, where claim 20 improperly depends on claim 14, while claim 15 depends on claim 11.

b. Claim 2 recites the limitation, "single integrate circuit" on its last line. Please correct the claim language to more clearly read, "single integrated circuit".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 15-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 15 recites the limitation "the string of bits" in its first line. There is insufficient antecedent basis for this limitation in the claim. Dependent claim 16 contains all of the limitations of its parent claims, and thus is rejected for the same reasons as above.

***Claim Rejections - 35 USC § 102***

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Barry et al., U.S. Patent No. 6,397,324.

12. Regarding claims 1 and 25, taking claim 1 as exemplary, Barry has taught a method for execution by a microprocessor in response to receiving a single instruction (see "S2TBL" on Col.12 lines 13-27), the method comprising:

a. Receiving a first plurality of numbers (see An/Ri of Fig.4 or An/Rz of Fig.8) and a second plurality of numbers (see Rs of Fig.4 or Rte/Rto of Fig.8), each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables (431/433 of Fig.4) (see Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction, which is the STBL

instruction modified to perform two look-up table stores (see Col.9 lines 53-62), specifies two base registers (An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (see Col.12 lines 14-27). The S2TBL instruction further specifies two pieces of data denoted by even and odd addresses (each piece of data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (see Col.10 lines 5-20).

b. Replacing simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers (see Col.9 lines 41-62 and Col.12 lines 14-27),

c. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (see "S2TBL" on Col.12 lines 13-27).

13. Claim 25 is nearly identical to claim 1, differing in its method being comprised upon a machine-readable medium (see Barry, Fig.8A), but encompassing the same scope as claim 1. Therefore, claim 25 is rejected for the same reasons as claim 1.

14. Regarding claims 2 and 26, taking claim 2 as exemplary, Barry has taught a method as in claim 1, wherein:

a. The first plurality of numbers are received from a first entry in a register file (see Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction specifies, using even/odd addressing, two base registers (An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers

(a plurality of "numbers") to an entry in one of the look-up tables (see Col.12 lines 14-27). Thus, the execution unit "receives" the first plurality of numbers from a first entry in a register file (An + Rz).

b. The second plurality of numbers are received from a second entry in the register file (see Col.9 line 25 – Col.10 line 20 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction specifies two pieces of data denoted by odd and even addresses (each data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (see Col.10 lines 5-20)

c. Wherein the microprocessor is a media processor integrated with a memory controller (485 of Fig.4) on a single integrated circuit (see Fig.4).

15. Claim 26 is nearly identical to claim 2, differing in its parent claim, but encompassing the same scope as claim 2. Therefore, claim 26 is rejected for the same reasons as claim 2.

16. Regarding claims 3 and 27, taking claim 3 as exemplary, Barry has taught a method as in claim 2, wherein the single instruction specifies indices of the first (An and Rz of Fig.8, see also Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27) and second entries (Rt in Fig.8, see also Col.9 line 25 – Col.10 line 20 and Col.11 line 64 – Col.12 line 27) in the register file.

17. Claim 27 is nearly identical to claim 3, differing in its parent claim, but encompassing the same scope as claim 3. Therefore, claim 27 is rejected for the same reasons as claim 3.

18. Regarding claims 4 and 28, taking claim 4 as exemplary, Barry has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Replacing at least one entry in at least one of a plurality of look-up units (431/433 of Fig.4) in a microprocessor unit with at least one number using a Direct Memory Access (DMA) controller (see Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction, which is the STBL instruction modified to perform two look-up table stores (see Col.9 lines 53-62), specifies two base registers (An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (see Col.12 lines 14-27). The S2TBL instruction further specifies two pieces of data denoted by even and odd addresses (each piece of data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (see Col.10 lines 5-20). The entries are updated via the memory interface unit (485 of Fig.4), which is a DMA controller (see Col.7 lines 50-62).

b. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (see "S2TBL" on Col.12 lines 13-27).

19. Claim 28 is nearly identical to claim 4, differing in its parent claim, but encompassing the same scope as claim 4. Therefore, claim 28 is rejected for the same reasons as claim 4.

20. Regarding claims 5 and 29, taking claim 5 as exemplary, Barry has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Replacing at least one entry for each of a plurality of look-up units (431/433 of Fig.4) in a microprocessor with a plurality of numbers using a Direct Memory Access (DMA) controller (see Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction, which is the STBL instruction modified to perform two look-up table stores (see Col.9 lines 53-62), specifies two base registers (An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (see Col.12 lines 14-27). The S2TBL instruction further specifies two pieces of data denoted by even and odd addresses (each piece of data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (see Col.10 lines 5-20). The entries are updated via the memory interface unit (485 of Fig.4), which is a DMA controller (see Col.7 lines 50-62).

b. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (see "S2TBL" on Col.12 lines 13-27).

21. Claim 29 is nearly identical to claim 5, differing in its method being comprised upon a machine-readable medium (see Barry, Fig.8A), but encompassing the same scope as claim 5. Therefore, claim 29 is rejected for the same reasons as claim 5.

22. Regarding claims 6 and 30, taking claim 6 as exemplary, Barry has taught a method as in claim 5, wherein a single index encoded in the instruction specifies a location of the at least one entry in the plurality of look-up units (see Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction, which is the STBL instruction modified to perform two look-up table stores (see Col.9 lines 53-62), specifies two base registers (An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (see Col.12 lines 14-27). Thus, each instruction contains an encoded pointer that is an index into a corresponding look-up table.

23. Claim 30 is nearly identical to claim 6, differing in its parent claim, but encompassing the same scope as claim 6. Therefore, claim 30 is rejected for the same reasons as claim 6.

24. Regarding claims 7 and 31, taking claim 7 as exemplary, Barry has taught a method as in claim 5, wherein a single index encoded in the instruction specifies a total number of the at least one entry for each of a plurality of look-up units (see Col.10 line 62 - Col.11 line 48). Here, Barry supports three instructions (STBL, S2TBL and S4TBL) that each specify a different number of entries in the look-up tables based on the instruction itself.

25. Claim 31 is nearly identical to claim 7, differing in its parent claim, but encompassing the same scope as claim 7. Therefore, claim 31 is rejected for the same reasons as claim 7.

26. Regarding claims 8 and 32, taking claim 8 as exemplary, Barry has taught a method as in claim 5, wherein a source address of the plurality of numbers is specified in

an entry of a register file (see Col.12 lines 14-28). The S2TBL instruction specifies two pieces of data denoted by even and odd addresses (each piece of data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (see Col.10 lines 5-20). Thus because the index of the register file is specified in the instruction, and the source address of the plurality of numbers is the index of that entry in the register file, the source address of the plurality of numbers is specified in an entry in the register file.

27. Claim 32 is nearly identical to claim 8, differing in its parent claim, but encompassing the same scope as claim 8. Therefore, claim 32 is rejected for the same reasons as claim 8.

28. Regarding claims 9 and 33, taking claim 9 as exemplary, Barry has taught a method as in claim 8, wherein the single instruction specifies an index of the entry in the register file (see Col.12 lines 14-28). The S2TBL instruction specifies the register indices (see Fig.8A) of two pieces of data denoted by even and odd addresses (each piece of data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (see Col.10 lines 5-20).

29. Claim 33 is nearly identical to claim 9, differing in its parent claim, but encompassing the same scope as claim 9. Therefore, claim 33 is rejected for the same reasons as claim 9.

30. Regarding claims 10 and 34, taking claim 10 as exemplary, Barry has taught a method as in claim 5, wherein an identity number encoded in the single instruction specifies the DMA controller (see Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27).

Here, the S2TBL instruction specifies two base registers (An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers to an entry in one of the look-up tables (see Col.12 lines 14-27). Because the pointers are "encoded" in the instruction, and because all accesses to the look-up tables use the DMA controller (see Col.7 lines 50-62), the instruction inherently specifies the DMA controller.

31. Claim 34 is nearly identical to claim 10, differing in its parent claim, but encompassing the same scope as claim 10. Therefore, claim 34 is rejected for the same reasons as claim 10.

32. Regarding claims 11 and 35, taking claim 11 as exemplary, Barry has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving a plurality of numbers (see An/Rz of Fig.6). Here, the L2TBL instruction, which is the LTBL instruction modified to perform two look-up table look-ups (see Col.9 lines 53-62), specifies two base registers (An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (see Col.10 line 62 – Col.11 line 32).

b. Partitioning look-up memory into a plurality of look-up tables (see Col.7 lines 54-62 and Col.9 lines 63-67),

c. Look up simultaneously a plurality of elements from the plurality of look-up tables (431/433 of Fig.4), each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers (see Col.9 lines 41-67 and Col.12 lines 14-27). Here,

the above two pointers received point to elements in the look-up tables, and the L2TBL instruction subsequently reads the elements pointed to and stores them in a corresponding entry in the register file.

d. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (see "L2TBL" on Col.10 line 62 – Col.11 line 32).

33. Claim 35 is nearly identical to claim 11, differing in its method being comprised upon a machine-readable medium (see Barry, Fig.8A), but encompassing the same scope as claim 11. Therefore, claim 35 is rejected for the same reasons as claim 11.

34. Regarding claims 12 and 36, taking claim 12 as exemplary, Barry has taught a method as in claim 11, wherein the receiving a plurality of numbers comprises:

a. Partitioning a string of bits into a plurality of segments to generate the plurality of numbers (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies a string of bits within the Rz register, and partitions them into two segments of data, Rze and Rzo based on the even and odd source register address.

35. Claim 36 is nearly identical to claim 12, differing in its parent claim, but encompassing the same scope as claim 12. Therefore, claim 36 is rejected for the same reasons as claim 12.

36. Regarding claims 13 and 37, taking claim 13 as exemplary, Barry has taught a method as in claim 12, wherein the single instruction specifies format information in which the plurality of numbers are stored in the string of bits (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies a string of bits within the Rz register (see

Fig.6A), and formats them into two segments of data, Rze and Rzo based on the even and odd source register address (see Col.10 line 62 – Col.11 line 32).

37. Claim 37 is nearly identical to claim 13, differing in its parent claim, but encompassing the same scope as claim 13. Therefore, claim 37 is rejected for the same reasons as claim 13.

38. Regarding claims 14 and 38, taking claim 14 as exemplary, Barry has taught a method as in claim 11, wherein the look-up memory comprises a plurality of look-up units (431/433 of Fig.4), and wherein said partitioning look-up memory comprises:

a. Configuring the plurality of look-up units into the plurality of look-up tables (see Col.7 lines 54-62 and Col.9 lines 63-67).

39. Claim 38 is nearly identical to claim 14, differing in its parent claim, but encompassing the same scope as claim 14. Therefore, claim 38 is rejected for the same reasons as claim 14.

40. Regarding claims 15 and 39, taking claim 15 as exemplary, Barry has taught a method as in claim 11, wherein the string of bits is received from an entry of a register file (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies a string of bits within the Rz register (see Fig.6A), and formats them into two segments of data, Rze and Rzo based on the even and odd source register address (see Col.10 line 62 – Col.11 line 32).

41. Claim 39 is nearly identical to claim 15, differing in its parent claim, but encompassing the same scope as claim 15. Therefore, claim 39 is rejected for the same reasons as claim 15.

42. Regarding claims 16 and 40, taking claim 16 as exemplary, Barry has taught a method as in claim 15, wherein the single instruction specifies an index of the entry (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies a string of bits within the Rz register (see Fig.6A), and formats them into two segments of data, Rze and Rzo based on the even and odd source register address (see Col.10 line 62 – Col.11 line 32).

43. Claim 40 is nearly identical to claim 16, differing in its parent claim, but encompassing the same scope as claim 16. Therefore, claim 40 is rejected for the same reasons as claim 16.

44. Regarding claims 17 and 41, taking claim 17 as exemplary, Barry has taught a method as in claim 11, further comprising:

a. Storing the plurality of elements in an entry of the register file (see Col.10 line 62 – Col.11 line 32).

45. Claim 41 is nearly identical to claim 17, differing in its parent claim, but encompassing the same scope as claim 17. Therefore, claim 41 is rejected for the same reasons as claim 17.

46. Regarding claims 18 and 42, taking claim 18 as exemplary, Barry has taught a method as in claim 17, wherein the single instruction specifies an index of the entry (see Rt of Fig.6A and Col.10 line 62 – Col.11 line 32).

47. Claim 42 is nearly identical to claim 18, differing in its parent claim, but encompassing the same scope as claim 18. Therefore, claim 42 is rejected for the same reasons as claim 18.

48. Regarding claims 19 and 43, taking claim 19 as exemplary, Barry has taught a method as in claim 17, wherein the single instruction specifies format information in which the plurality of elements are stored in the entry (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies that the plurality of data entries are stored at even and odd addresses into the register file, thus specifying the format.

49. Claim 43 is nearly identical to claim 19, differing in its parent claim, but encompassing the same scope as claim 19. Therefore, claim 43 is rejected for the same reasons as claim 19.

50. Regarding claims 20 and 44, taking claim 20 as exemplary, Barry has taught a method as in claim 14, wherein each of the plurality of look-up units comprises 256 8-bit entries (see Col.10 line 62 - Col.11 line 48). Here, Barry supports look-up table sizes of 256 (see Col.11 line 44) and 64000 (see Col.11 lines 13-14) entries, each entry being an 8, 16 or 32-bit entry.

51. Claim 44 is nearly identical to claim 20, differing in its parent claim, but encompassing the same scope as claim 20. Therefore, claim 44 is rejected for the same reasons as claim 20.

52. Regarding claims 21 and 45, taking claim 21 as exemplary, Barry has taught a method as in claim 11, wherein the single instruction specifies a total number of entries contained in each of the plurality of look-up tables (see Col.10 line 62 - Col.11 line 48). Here, Barry supports three instructions (STBL, S2TBL and S4TBL) that each specify a different number of entries in the look-up tables, as well as the size of each entry.

53. Claim 45 is nearly identical to claim 21, differing in its parent claim, but encompassing the same scope as claim 21. Therefore, claim 45 is rejected for the same reasons as claim 21.

54. Regarding claims 22 and 46, taking claim 22 as exemplary, Barry has taught a method as in claim 21, wherein the total number of entries is one of:

a. 256 (see Col.11 line 44),

b. 512

c. 1024.

55. Here, Barry supports look-up table sizes of 256 (see Col.11 line 44) and 64000 (see Col.11 lines 13-14) entries, each entry being an 8, 16 or 32-bit entry. Because the claim has been written in the alternative format, only one of the alternative limitations is required to be taught by the prior art, and thus Barry has taught the limitations of claim 22.

56. Claim 46 is nearly identical to claim 22, differing in its parent claim, but encompassing the same scope as claim 22. Therefore, claim 46 is rejected for the same reasons as claim 22.

57. Regarding claims 23 and 47, taking claim 23 as exemplary, Barry has taught a method as in claim 11, wherein the single instruction specifies a total number of bits used by each entry contained in the plurality of look-up tables (see Col.12 lines 14-28). Here, the "size" field of the S2TBL instruction (see Fig.8A and Col.12 lines 66-67) specifies whether the instruction is to use dual word, word, dual-half word or dual byte data is used in the look-up table entries (see Col.10 line 62-Col.11 lines 27 and Col.12 lines 14-28).

58. Claim 47 is nearly identical to claim 23, differing in its parent claim, but encompassing the same scope as claim 23. Therefore, claim 47 is rejected for the same reasons as claim 23.

59. Regarding claims 24 and 48, taking claim 24 as exemplary, Barry has taught a method as in claim 21, wherein the total number of bits is one of:

a. 8 ("two bytes" in Col.12 lines 14-28),

b. 16 ("two halfwords" in Col.12 lines 14-28),

c. 24.

60. Because the claim has been written in the alternative format, only one of the alternative limitations is required to be taught by the prior art, and thus Barry has taught the limitations of claim 24.

61. Claim 48 is nearly identical to claim 24, differing in its parent claim, but encompassing the same scope as claim 24. Therefore, claim 48 is rejected for the same reasons as claim 24.

***Conclusion***

62. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

63. Ansari, U.S. Patent No. 6,553,486, has taught load and store vector instructions for reading from and storing to a look-up table.

64. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

65. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
8/17/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100